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09/667,046	09/21/2000	Steven A. Lytle	LYTLE 18	8375

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HITT GAINES P.C.
P.O. BOX 832570
RICHARDSON, TX 75083

EXAMINER
VU, HUNG K

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 21

Application Number: 09/667,046
Filing Date: September 21, 2000
Appellant(s): LYTLE, STEVEN A.

Jimmy L. Heisz
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/30/03.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 21, 24 and 25, and claims 29 and 30 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,177,340	YOO ET AL.	01-2001
6,163,067	INOHARA ET AL.	12-2000

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 21 and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang (PN 6,127,260).

Huang discloses, as shown in Figure 10, a semiconductor device comprising,

a first interconnect metal (13) located on or in a first interlevel dielectric layer (20);

a second interconnect metal (lower portion of 44) located on or in a second interlevel dielectric layer (31), the second interlevel dielectric layer located over the first interlevel dielectric layer;

a third interconnect metal (upper portion of 44) located on or in a third interlevel dielectric layer (37), the third interlevel dielectric layer located over the second dielectric layer;

a via (42a) located through the second and third interlevel dielectric layers and connecting the first and third interconnect metals, the via being void of a landing pad between the second and third interlevel dielectric layers.

With regard to Claim 24, Huang discloses the via is a passing metal via with no passing metal feature.

With regard to Claim 25, Huang discloses the device further including transistors wherein the first metal feature is located over the transistors and interconnects the transistors to form an operative integrated circuit.

2. Claims 21 and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoo et al. (PN 6,177,340).

Yoo et al. discloses, as shown in Figure 20, a semiconductor device comprising,

a first interconnect metal (9) located on or in a first interlevel dielectric layer (19);

a second interconnect metal (31) located on or in a second interlevel dielectric layer (23), the second interlevel dielectric layer located over the first interlevel dielectric layer;

a third interconnect metal (55) located on or in a third interlevel dielectric layer (49), the third interlevel dielectric layer located over the second dielectric layer;

a via (27,51) located through the second and third interlevel dielectric layers and connecting the first and third interconnect metals, the via being void of a landing pad between the second and third interlevel dielectric layers.

With regard to Claim 24, Yoo et al. discloses the via is a passing metal via with no passing metal feature.

With regard to Claim 25, Yoo et al. discloses the device further including transistors wherein the first metal feature is located over the transistors and interconnects the transistors to form an operative integrated circuit.

3. Claims 29-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Inohara et al. (PN 6,163,067).

Inohara et al. discloses, as shown in Figures 12-14, a semiconductor device comprising,

a first metal feature (25) located on a semiconductor surface;

a first etch stop layer (13a) located on the first metal feature;

a first interlevel dielectric layer (13b) located on the first etch stop layer;

a second etch stop layer (14a) located on the first interlevel dielectric layer;

a second interlevel dielectric layer (14b) located on the second etch stop layer;

an unsegmented via (32) located through the first and second etch stop layers and interlevel dielectric layers, the unsegmented via extending to and contacting the first metal feature and being void of a landing pad between the first and second interlevel dielectric layers; (Figure 21)

a second metal feature (16b) located adjacent the unsegmented via and extending through the second interlevel dielectric layers and the second etch stop layer and terminating at the first interlevel dielectric layer;

a dual damascene structure adjacent the second metal feature and having a damascene trench portion (16) extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer and further including a damascene via portion (16c) extending through the first interlevel dielectric layer and the first etch stop layer and connecting the trench portion to the first metal feature.

With regard to Claim 30, Inohara et al. discloses the unsegmented via is a passing metal via with no passing metal feature.

(11) Response to Argument

The examiner interprets Figure 8 of the present invention as follow:

a first interconnect metal – formed in via 820

a first interlevel dielectric layer – layers 830 and 832

a second interconnect metal – formed in via 838

a second interlevel dielectric layer – layer 834

a third interconnect metal – formed in via below layer 110

a third interlevel dielectric layer – layer 830

Appellant argued the metal silicide 13 disclosed in Huang is not an interconnect metal because it does not provide a connection between the other features. This argument is not convincing because Huang clearly discloses, as shown in Figure 10, the metal silicide 13 provides the connection between the layer 12 and the layer 44.

Appellant argued the lower metal plug structure 44 in Huang is a via, not an interconnect metal because interconnect structures are not formed in vias. This argument is not convincing because the features upon which Appellant relies (i.e., interconnect structures are not formed in vias) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations fro them specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Note that the present invention also discloses, as shown in Figure 8, the second metal interconnect is formed in the via 838.

Appellant argued the via is a metal filled opening between various layers of a semiconductor device that provides electrical connection between layers, and the via 42a in Huang is the narrow empty opening and does not provide electrical connection between the layers. This argument is not convincing because the features upon which Appellant relies (i.e., the via is a metal filled opening between various layers of a semiconductor device that provides electrical connection between the layers) are not recited in the rejected claim(s).

Appellant argued the titanium silicide 9 disclosed in Yoo is not an interconnect metal because it does not provide a connection between the other features. This argument is not convincing

because Yoo clearly discloses, as shown in Figures 3, 11 and 20, the titanium silicide 9 provides the connection between the layer 27 and the source/drain region 5b/7b.

Appellant argued the tungsten plug 31 in Yoo is a via, not an interconnect metal because interconnect structures are not formed in vias. This argument is not convincing because the features upon which Appellant relies (i.e., interconnect structures are not formed in vias) are not recited in the rejected claim(s). Note that the present invention also discloses, as shown in Figure 8, the second metal interconnect is formed in the via 838.

Appellant argued the tungsten plug 55 in Yoo is a via, not an interconnect metal because interconnect structures are not formed in vias. This argument is not convincing because the features upon which Appellant relies (i.e., interconnect structures are not formed in vias) are not recited in the rejected claim(s).

Appellant argued the via is a metal filled opening between various layers of a semiconductor device that provides electrical connection between layers, and the contact hole openings 27 and 51 in Yoo is the opening and does not provide electrical connection between the layers. This argument is not convincing because the features upon which Appellant relies (i.e., the via is a metal filled opening between various layers of a semiconductor device that provides electrical connection between the layers) are not recited in the rejected claim(s).

Appellant argued the silicide layer 25 in Inohara is located in source/drain regions 22a/22b and is not located on a semiconductor surface. This argument is not convincing because Inohara discloses, as shown in Figure 13, the silicide layer 25 is located on a portion of the semiconductor surface 11.

Appellant argued the stopper film 13a is located over and laterally adjacent the silicide layer 25 and is not located on the silicide layer 25. This argument is not convincing because the word "on" does not necessary mean directly on or directly above.

Appellant argued the via is a metal filled opening between various layers of a semiconductor device that provides electrical connection between layers, and the contact hole 32 in Inohara is an empty, un-filled opening through multiple layers is not a via because it does not provide electrical connection between the layers. This argument is not convincing because the features upon which Appellant relies (i.e., the via is a metal filled opening between various layers of a semiconductor device that provides electrical connection between the layers) are not recited in the rejected claim(s).

Appellant argued Inohara fails to disclose either an unsegmented via or a second metal feature. This argument is not convincing because Inohara clearly discloses, as shown in Figures 12-14, the unsegmented via 32 and the second metal feature 16a&16b, as claimed. Note that the second metal feature 16a&16b is located directly above layer 21 and adjacent the unsegmented via 32.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Hung Vu
Patent Examiner

Vu
September 4, 2003

Conferees
Tom Thomas
Olik Chaudhuri
Hung Vu

CHARLES W GAINES
HITT GAINES & BOISBRUN PC
P O BOX 832570
RICHARDSON, TX 75083